Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **QL**
2. **QM**
3. **QN**
4. **QF**
5. **QE**
6. **QG**
7. **QD**
8. **GND**
9. **CLKO**
10. **N. CLKO**
11. **CLK 1**
12. **CLR**
13. **QI**
14. **QH**
15. **QJ**
16. **VCC**

**MASK**

**REF**

**2 1 16 15**

**14**

**13**

**12**

**11**

**10**

**3**

**4**

**5**

**6 7 8 9**

**HC**

**4060G**

**Top Material: Al**

**Backside Material: Si Ni**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VCC (or leave FLOATING)**

**Mask Ref: HC4060G**

**APPROVED BY: DK DIE SIZE .072” X .091” DATE: 8/26/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: 54HC4060**

**DG 10.1.2**

#### Rev B, 7/19/02